Remarks

In furtherance of the Request for Continued Examination filed herewith, Applicants respectfully request consideration of the foregoing amendments, which are hereby submitted in accordance with 37 C.F.R. § 1.114. Upon entry of the foregoing amendment, claims 1, 9, 18, 36-41, 43-48, 58-62, and 68-83 are pending in the application, with claims 1, 18, 58, 68, 76, and 83 being the independent claims. Claims 68, 76, and 83 are sought to be amended. These changes introduce no new matter, and their entry is respectfully requested.

Support for the amendment of claims 68, 76, and 83 is found at, for example, p. 11, lines 5-8 , p. 41, line 18 through p. 42, line 10, p. 44, lines 9-12, and in FIG. 6 of the specification.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Interview

Applicants thank the Examiner for discussing the current office action with the undersigned on June 20, 2006. The Examiner discussed his rationale for combining the Heene and Larsen references in rejecting the pending claims under 35 USC § 103. The undersigned contended that a person of skill in the art would not have thought to consider the Heene reference, because this reference concerns the comparison of instruction addresses for the purpose of calling a patch for existing code, while the present invention concerns the

comparison of instruction addresses for the purpose of switching instruction set architectures. Because the two references address different technical problems, the undersigned contended that a person of skill in the art would not have been motivated to combine the Heene and Larsen references. The undersigned also discussed the possibility of amending the claims in the manner presented above.

Allowable Claims

The Office Action states that claims 1, 9, 19, 36-41, 43-48, and 58-62 are allowable. Applicants thank the Examiner for his consideration of these claims.

Rejections Under 35 U.S.C. § 103

The Examiner has rejected claim 68 as being obvious over U.S. Patent 5,115,500 ("Larsen") in view of U.S. Patent 4,802,119 ("Heene"). This claim has been amended as described above. Claim 68 now recites:

68. Instruction Set Architecture (ISA) selection logic within a CPU for selecting an ISA decoding mode for a program instruction, the selection logic comprising:

a plurality of boundary address registers for storing boundary addresses that partition an address space into a plurality of address ranges, each of the plurality of address ranges corresponding to one of a plurality of ISA decoding modes; and

an ISA mode controller, coupled to the plurality of boundary address registers, that includes address evaluation logic,

wherein the ISA mode controller

receives a complete_address of a program instruction to be decoded,

compares, in parallel, the complete address to boundary addresses stored in the plurality of boundary address registers, and

determines an ISA decoding mode for the program instruction based upon the comparison of the complete address to the boundary addresses.

This claim now includes features that are neither disclosed nor suggested by either Larsen or Heene. For at least this reason, claim 68 as amended is not rendered obvious over any reasonable combination of these references.

The Examiner has also rejected claims 69-75 as being obvious over Larsen in view of Heene. The rejection of each of these claims was premised on the earlier rejection of independent claim 68, upon which claims 69-75 depend. Each of these dependent claims includes all features of claim 68 as amended. Claim 68 as amended includes features that are neither disclosed nor suggested by either Heene or Larsen. For at least this reason, none of claims 69-82 is rendered obvious by any reasonable combination of these references.

The Examiner has rejected claim 76 as being obvious over Larsen in view of Heene. This claim has been amended as described above. Claim 76 now recites:

76. A multiple-ISA mode processor, comprising:

an ISA mode controller that includes address evaluation logic;

a plurality of boundary address registers, coupled to the ISA mode controller; and

an instruction decoder, coupled to the ISA mode controller,

wherein the ISA mode controller

receives a complete address of a program instruction to be decoded,

compares, in parallel, the complete address to boundary addresses stored in the plurality of boundary address registers that partition an address space of the processor into a plurality of address ranges,

determines an ISA decoding mode corresponding to one of the plurality of address ranges for the program instruction based upon the comparison of the complete address to the boundary addresses, and

provides the ISA decoding mode for the program instruction to the instruction decoder.

This claim now includes features that are neither disclosed nor suggested by either Larsen or Heene. For at least this reason, claim 76 as amended is not rendered obvious over any reasonable combination of these references.

The Examiner has also rejected claims 77-82 as being obvious over Larsen in view of Heene. The rejection of each of these claims is premised on the earlier rejection of independent claim 76, upon which claims 77-82 depend. Each of these dependent claims includes all features of claim 76 as amended. Claim 76 now contains features that are neither disclosed nor suggested by either Heene or Larsen. For at least this reason, none of claims 77-82 is rendered obvious by any reasonable combination of these references.

The Examiner has also rejected claim 83 as being obvious over Larsen in view of Heene. This claim has been amended as described above. Claim 83 now reads as follows:

83. A method for determining ISA decoding modes for program instructions of a multiple-ISA application program running on a processor, wherein the application program includes instructions associated with a first ISA mode requiring a first amount of memory space and instructions associated with a second ISA mode requiring a second amount of memory space, and wherein the processor includes a plurality of boundary address registers and an ISA mode controller coupled to the plurality of boundary address registers, the method comprising:

(1) storing application program instructions associated with the first ISA mode in memory beginning at a first memory address;

(2) writing the first memory address to a first boundary address register of the plurality of boundary address registers, wherein the first memory address acts as a first boundary address that partitions the memory and creates a first memory address range;

(3) storing application program instructions associated with the second ISA mode in memory beginning at a second memory address;

(4) writing the second memory address to a second boundary address register of the plurality of boundary address registers, wherein the second memory address acts as a second boundary address that partitions the memory and creates a second memory address range;

(5) retrieving a program instruction form a third memory address;

(6) comparing, in parallel, the complete third memory address with the first memory address in the first boundary address register and the second memory address in the second boundary address register to determine whether the third memory address corresponds to the first memory address range or the second memory address range;

(7) generating, if the third memory address corresponds to the first memory address range, a first ISA mode indicator output with the ISA mode controller; and

(8) generating, if the third memory address corresponds to the second memory address range, a second ISA mode indicator output with the ISA mode controller.

This claim now includes features that are neither disclosed nor suggested by either Larsen or Heene. For at least this reason, claim 83 as amended is not rendered obvious over any reasonable combination of these references.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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